REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated April 9, 2003. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1, 3-9, 11-13, and 15-22 are under consideration in this application. Claims 2, 10 and 14 are being cancelled without prejudice or disclaimer. Claims 20-22 were withdrawn. Claims 1, 3, 7-9, 12 and 15-19 are being amended, as set forth above and in the attached marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim Applicants' invention. New claims 23-25 are being added to recited other embodiments described in the specification.

Additional Amendments

The claims, the specification, and Fig. 10 are being amended to correct formal errors and/or to better disclose or describe the features of the present invention as claimed. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Formality Rejections

The drawings were objected to and has requested correction thereof. The abstract was objected to as exceeding 150 words and as being in an improper format. Claims 16-17 were objected to due to their improper multiple dependent format, and therefore these two claims were not examined, and claims 1-19 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. As indicated, the specification and the claims have been amended as required by the Examiner. Accordingly, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Prior Art Rejections

Claims 1-17 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,300,835 to Assar et al. (hereinafter "Assar"), and claims 18-19 were rejected under 35 U.S.C. § 103(a) as being rendered obvious by Assar. The prior art references of Kim et al. (6,501,306), Nakashiro et al. (5,723,986), and Ovens et al. (6,351,173), were cited as being pertinent to the present application. These rejections have been carefully considered, but are most respectfully traversed.

The level conversion circuit (Fig. 1) of the invention, as now recited in claim 1, comprises: a first circuit (11 and 12 of Fig. 1) including a first input terminal (IN) for receiving a first signal having a first signal amplitude, a first output terminal (line of signal "a") for supplying a second signal having a second signal amplitude greater than said first signal amplitude and being in the same phase as said first signal, and a second output terminal (line of signal "b") for supplying a third signal having said second signal amplitude and being in a phase reverse to said first signal; and a second circuit (13, 14, 15) including a first p-channel type MOS transistor (Qp5), a second p-channel type MOS transistor (Qp6), a first n-channel type MOS transistor (Qn5), a second n-channel type MOS transistor (Qn6) and, a third output terminal (OUT), <u>a source of said first p-channel type MOS transistor (Qp5) being coupled to a first voltage terminal VDD2, a drain of said first p-channel type MOS transistor (Qp5) being coupled to a source of said second p-channel type MOS transistor (Qp6), a drain of said second p-channel type MOS transistor (Qp6) and a drain of said first n-channel type MOS transistor (Qn5) being coupled to said third output terminal (OUT), a source of said first n-channel type MOS transistor (Qn5) being coupled to a drain of said second n-channel type MOS transistor (Qn6) and a source of said second n-channel type MOS transistor (Qn6) being coupled to a second voltage terminal VSS</u>. In particular, <u>the second circuit is configured to form</u> a fourth signal outputted from said third output terminal, <u>said fourth signal</u> having <u>a signal level of</u> said second signal amplitude and <u>changing on the basis of the signal variation of said second signal</u> ("a" of Fig. 1 and Fig. 2) supplied from said first output terminal of said first circuit <u>or of said third signal</u> ("b" of Fig. 1 and Fig. 2) supplied from said second output terminal of said first circuit <u>whichever signal level changes faster to very a logical threshold of said second circuit so as to accelerate the variation of said fourth signal</u> ("*the second circuit may as well be so configured as to cause the state of the first p-channel type MOS transistor or the second n-channel type MOS transistor in response to a variation of the second signal or the third signal supplied from the first circuit, whichever is faster. This results in a variation of the thresholds of the first p-channel type MOS transistor and the second n-channel type MOS transistor by the*

substrate bias effect, making it possible to avoid a slowdown in output signal variation" page 10, lines 9-17; page 7, lines 3-11).

The first circuit, as recited in claim 7, comprises: a first inverter (11 of Fig. 1; page 7, last line) for logically inverting said first signal; a first node for receiving the output signal of said first inverter; a third n-channel type MOS transistor (Qn2); a fourth n-channel type MOS transistor (Qn3) whose gate terminals are connected respectively to said first input terminal and said first node; a third p-channel type MOS transistor (Qp2) whose source-drain path is connected in series to said third n-channel type MOS transistor and whose gate terminal is connected to the drain terminal of said fourth n-channel type MOS transistor; and a fourth p-channel type MOS transistor (Qp3) whose source-drain path is connected in series to said fourth n-channel type MOS transistor and whose gate terminal is connected to the drain terminal of said third n-channel type MOS transistor, said first output terminal being connected to the drain terminal said fourth n-channel type MOS transistor, said second output terminal being connected to the drain terminal of said third n-channel type MOS transistor. The second circuit comprises a second inverter (13) for logically inverting said third signal being connected to said second output terminal. The second circuit, as recited in claim 9, further comprises a third inverter (15 in Fig. 1, page 9. line 10) to control said first p-channel type MOS transistor and second n-channel type MOS transistor according to the second signal supplied from said first output terminal of said first circuit or the output signal of said second inverter, whichever is slower in signal variation. "*This configuration makes it possible to shift the first p-channel type MOS transistor and the second n-channel type MOS transistor to an on/off state without delay after the fourth signal supplied from the second circuit varies and to prepare for the next signal variation* (page 9, lines 15-19)." As recited in claim 20, the logical threshold of said second circuit is determined by (i) relative gate widths (e.g., page 24, lines 21-24; page 25, lines 1-6; page 30, lines 1-9; "*Wn3 is greater than Wp3, the signal variation at the node n2 from a high level to a low level is faster than in the conventional level conversion circuit shown in Fig. 10*" page 33, lines 6-8; "*the MOSFETs Qn2, Qn3, Qp5, Qp6 and Qn6 are designed to be somewhat greater in the gate width than other elements*" page 51, lines 10-13 & Fig. 13) or (ii) relative gate width/gate length ratios (e.g., page 7, line 12; page 22, lines 2-9) of MOS transistors in said first and second circuits.

The invention is also directed to a generalized level conversion circuit of the invention, as now recited in claim 12, by eliminating the limitation of the physical MOS transistor arrangement of the second circuit from claim 1. The invention is also directed to a semiconductor integrated

circuit, as now recited in claim 18, comprising a pair of the level conversion circuits as now recited in claim 12.

The invention is further directed to a level conversion circuit, as now recited in claim 15, comprising: a first circuit including a first input terminal for receiving a first signal having a first signal amplitude, a first output terminal for supplying a second signal having a second signal amplitude greater than said first signal amplitude and being in the same phase as said first signal, and a second output terminal for supplying a third signal having said second signal amplitude and being in a phase reverse to said first signal; and a second circuit configured to form a fourth signal outputted from a third output terminal, said fourth signal having a signal level of said second signal amplitude and changing on the basis a variation of said second signal supplied from said first output terminal of said first circuit or of said third signal supplied from said second output terminal of said first circuit whichever signal level changes faster. In particular, a number of MOS transistor stages gone via by a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said first output terminal **is equal** (page 6, line 11) **to** a number of MOS transistor stages gone via by a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said second output terminal **as three** ("signal transmission is accomplished at even higher speed" than more MOS transistor stages, page 16, lines 7-8), wherein a stage of said MOS transistor stages (page 6, lines 4-5) is defined as a gate-drain path or a gate-source path of a MOS transistor in the level conversion circuit. "*This substantially equalizes the lengths of time taken by the signal in the same phase as the input signal and the signal in the reverse phase to the input signal to reach the second circuit, enabling the output signal to quickly vary not only at the leading edge but also the trailing edge of the input signal and the transmission speed of signals having different amplitudes to be raised* (page 6, lines 12-18)."

None of the cited prior art references teaches or suggests such "<u>a fourth signal having a signal level of said second signal amplitude and changing on the basis of the signal variation of said second signal or of said third signal whichever signal level changes faster to very a logical threshold of said second circuit so as to accelerate the variation of said fourth signal</u>" (claims 1 , 12 and 18); or "<u>a number of MOS transistor stages gone via by a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said first output terminal **is equal to** a number of MOS transistor stages gone via by a signal reaching said third output terminal of said second circuit from said first input terminal of said first circuit via said second output terminal **as three**</u>" (claim 15). Such arrangements *provide " a level conversion*

circuit in which the variation of output signals from a low level to a high level is substantially equal to that from a high level to a low level, and at the same time it is made possible to increase the operating speed of a system using a semiconductor integrated circuit having a level conversion circuit as its interfacing circuit (page 54, lines 14-19)". "*Accordingly, as indicated by broken line B in Fig. 11, the rise of the output of this level conversion circuit to a high level is faster than in the conventional level conversion circuit. The waveforms shown in Fig. 11 were obtained by the simulation of this level conversion circuit embodying the invention and the level conversion circuit embodying the prior art (page 33, last paragraph).*"

Assar simply does not disclose or suggest the above-mentioned characteristic features and the effect, while the other references fail to compensate for Assar's deficiencies.

Accordingly, Applicants contend that the cited conflicting teachings of the prior art references would not motivate their combination such that their combination would embody each and every feature of the present invention as now claimed in claims 1, 12, 15 and 18 from which claims 3-9, 11, 13, 15-17, and 19-22 depend. The difference is more than sufficient that the present invention as now claimed would not have been rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the

above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

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August 8, 2003

SPF/JCM/JT